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10/511,492	10/15/2004	Matthias Muth	DE02 0097 US	4584

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EXAMINER	
AMRANY, ADI	

ART UNIT	PAPER NUMBER
2836	

NOTIFICATION DATE	DELIVERY MODE
10/22/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/511,492	MUTH, MATTHIAS	
	Examiner	Art Unit	
	ADI AMRANY	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 August 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed August 11, 2009 have been fully considered but they are not persuasive. Applicant contends that Kawaguchi does not disclose the claimed logic circuit. The Examiner agrees with applicant that the battery voltage (via switch 9) or input voltage (via diode 18) are coupled to the ST terminal to turn on the DC/DC converter (6) (Remarks, page 6, 3rd paragraph). First, it noted that VR is the converter output voltage, not the voltage supplied to the ST terminal. Second, Vk is not a low voltage. Vk is the input voltage minus the voltage drop of diode (18). Third, applicant is incorrect is stating that the input voltage is not the same as the logic circuit voltage. Vk is the voltage of the charger minus the voltage drop of diode (18). Similarly, the voltage input to the DC/DC converter at HVI is the charger voltage minus the voltage drop of diode (16). Thus, Vk applied to ST and HVI are the same.

Next, applicant contends that the Kawaguchi logic circuit fails to provide the on-off signal to the converter is response to an idle state (Remarks, pages 6-7). The "on-off signal" does not specifically indicate which state the converter is to be placed into in response to the idle state. Does the converter turn on or turn off? As stated by the applicant, the Kawaguchi logic (ST) turns off the DC/DC converter (6) when loads are turned on (the reference actually uses the example of when lights are "left on", not just turned on). Conversely, this would mean that the DC/DC converter is turned on when the loads are not experiencing the conditions that would cause the DC/DC converter to turn off. Since turning the DC/DC converter off includes active loads, then turning the

DC/DC converter on would include off loads (i.e. circuit elements in the idle state). Thus, the Kawaguchi logic meets the broad limitation of providing on-off signals to the DC/DC converter in response to the idle state of the circuit elements.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art ("APA", specification, page 1) in view of Kawaguchi (US 5,793,189).

With respect to claim 1, APA discloses a circuit arrangement for a vehicle for generating at least two DC output voltages from at least one DC input voltage, wherein the DC output voltages are smaller than the DC input voltage, the circuit arrangement comprising: a voltage regulator for generating the DC output voltages to supply power to a set o circuit elements used for operating the vehicle from a voltage regulator input; a DC/DC converter for converting the DC input voltage to a lower voltage (page 1, lines 7-19). APA states that it is known from the state of the art to arrange a DC/DC converter preceding "such circuit arrangements." The circuit arrangements refers to page 1, lines 3-4, where APA states that voltage regulators are provided to generate Dc output voltages (plural).

APA does not expressly disclose the DC/DC converter can be switched on and off or that the logic circuit is powered by the DC input voltage.

Kawaguchi discloses a circuit arrangement for a vehicle (fig 1; col. 5-6) comprising a DC/DC converter (6) for converting the DC input voltage to a lower voltage (col. 5, lines 45-55), and a logic circuit (col. 5, lines 38-44) configured to provide the on-off signal to the DC/DC converter in response to an idle state in which the circuit elements are switched off (col. 7, line 57 to col. 8, line34), wherein the logic circuit is configured to receive the DC input voltage (via diode 18; col. 6, lines 57-65) to power the logic circuitry when the DC/DC converter is switched off. The Kawaguchi logic circuit recognizes the level of input voltage (which is based in part on the status of the loads) and turns the converter on/off accordingly.

The claim does not indicate if the converter is turned on or turned of when the idle state is detected. The broad limitation of providing an "on/off signal to the DC/DC converter in response to an idle state" is met by the Kawaguchi logic (ST input terminal).

APA and Kawaguchi are analogous because they are from the same field of endeavor, namely vehicle power distribution systems. At the time of the invention by applicant, it would have been obvious to one skilled in the art to combine the converter and regulator arrangement disclosed in APA with logic circuit on/off control and power input disclosed in Kawaguchi in order to reduce power consumption in the vehicle by turning off the converter when it is not needed (Kawaguchi, col. 12, lines 20-38).

With respect to claim 2, Kawaguchi discloses that the DC input voltage is used for energy supply of the arrangement (abstract).

With respect to claims 3-4, it would have been obvious to one skilled in the art to arrange any of the APA or Kawaguchi components on an integrated circuit, since it has been held that forming in one piece an article which has formerly been formed in two pieces and put together involves only routine skill in the art. *Howard v. Detroit Stove Works*, 150 U.S. 164 (1893). Placing components on an integrated circuit, as opposed to separate circuit boards, does not appear to affect their overall performance. Placing the components in one location is an aesthetic design choice in order to minimize space and clutter.

With respect to claim 5, APA and Kawaguchi combine to disclose the recited integrated circuit, as discussed above in the rejections of claims 1 and 4.

With respect to claim 6, Tamai disclose the DC input voltage has a value of approximately 42 volts (col. 4, lines 48-53) and the voltage supplied by the DC/DC converter has a value of approximately 12 volts (col. 4, lines 54-59). Further, it would be obvious to one skilled in the art to select any suitable input/output voltages for the DC/DC converter based on the end use of the device, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. *In re Boesch*, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

With respect to claims 7 and 14, Kawaguchi discloses that the logic circuit (ST node) is powered by the DC input voltage, as discussed above. The Kawaguchi logic circuit controls the on/off operation of the converter, but is never powered by the converter (voltage output node is VRO).

With respect to claims 8, 12 and 15, APA discloses that it is known in the art to configure the output voltages to be smaller than the lower voltage (the DC/DC converter output)(page 1, lines 1-4).

With respect to claims 9 and 16, Kawaguchi discloses a power supply (items 2, 10, 11, 16) configured to supply the DC input voltage. Kawaguchi discloses a battery (2) that is part of the power supply. As discussed in the rejection of claim 1, Kawaguchi was only relied upon to meet the limitations associated with the logic circuit (on/off operation and power input). Looking at Kawaguchi's figure 1, none of the components to the right (output side) of the converter (6) are relied upon the art rejection of the claims. APA discloses that the converter is coupled to a voltage regulator without the use of a battery. Thus, APA and Kawaguchi combine to disclose only one battery (Kawaguchi, item 2) which is part of the power supply.

With respect to claim 10, APA and Kawaguchi disclose the recited limitations, as discussed above in the rejections of claim 7 and 9.

With respect to claim 11, APA (page 1, lines 7-19) and Kawaguchi (col. 5, lines 45-55) disclose the DC/DC converter provides a lower voltage at the output, as discussed above in the rejection of claim 1.

With respect to claim 13, APA and Kawaguchi combine to disclose the recited limitations of a circuit arrangement, as discussed above in the rejection of claim 1. Claim 13 contains limitations identical to those presented in claim 1, except that claim 13 does not recite that the control circuitry is powered when the DC/DC converter is switched off. The references are analogous, as discussed above.

With respect to claim 17, Kawaguchi discloses the DC/DC converter turns on and off in response to the state of the circuit elements (col. 7, line 57 to col. 8, line 34), as discussed above in the rejection of claim 1.

Conclusion

4. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ADI AMRANY whose telephone number is (571)272-0415. The examiner can normally be reached on Mon-Thurs, from 10am-4pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jared Fureman can be reached on (571) 272-2800 x36. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

AA

10-16-09

/Stephen W Jackson/
Primary Examiner, Art Unit 2836